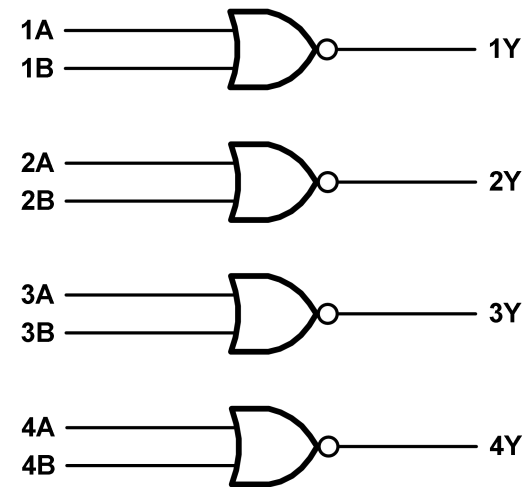


GT74LVC02

Quadruple 2-Input Positive-NOR Gate

1 Features	2 Application
<ul style="list-style-type: none"> - Operate from 1.65 V to 5.5 V - Supports 5-V VCC operation - Specified from -40°C to 125°C - Provides down translation to V_{CC} - Max t_{pd} of 4 ns at 3.3 V - ±24-mA output drive at 3.3 V 	<ul style="list-style-type: none"> - Personal digital assistant devices - AV receiver - MP3 player/recorder - Solid state drive (SSD): client and enterprise - Power: telecom/server AC/DC supply - TV: LCD/digital and high-definition (HDTV)

3 Description	Circuit Diagram
<p>This quadruple 2-input positive-NOR gate is designed for 1.65-V to 5.5-V V_{CC} operation.</p> <p>The GT74LVC02 performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.</p> <p>This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when the gate is powered down and its output is floating.</p>	

4 Revision History

Revision	Date	Note
Rev. A1.0	2023. 09. 02	Original Version
Rev. A1.1	2023. 12. 15	1.Updated Package Qty 2.Added Tape and Reel Information 3.Added Application Note
Rev. A1.2	2023. 12. 26	1.Added Marking 2.Added MSL
Rev. A1.3	2024. 01. 26	Updated Part Name

The latest datasheet version should be checked on the GTIC official website, as the company does not actively inform customers about updates to the datasheet.

5 Device Summary, Pin and Packages

Table 5-1. Device Summary⁽¹⁾

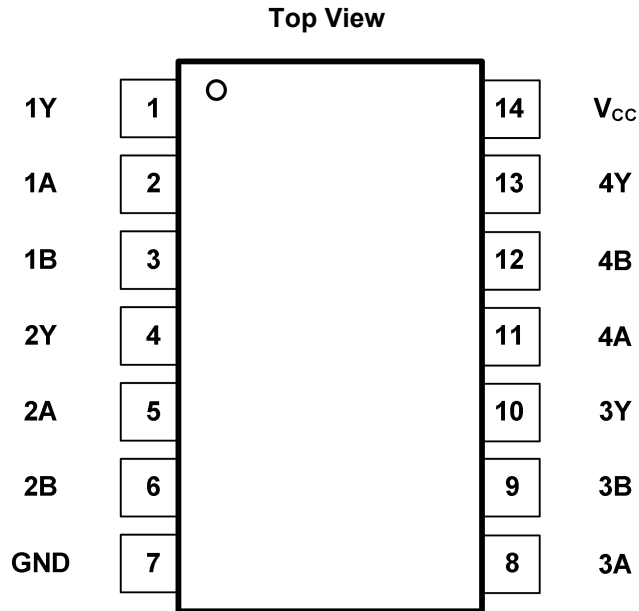
Serial Name	Part Name	Package	Body Size (Nom)	Marking ⁽²⁾⁽⁴⁾	MSL ⁽³⁾	Package Qty
GT74LVC02	GT74LVC02PD	SOP14/SOIC-14	8.65mm×3.90mm×1.75mm	GT74LVC02 XXXXXXX	3	Tape and Reel,4000
	GT74LVC02TD	TSSOP14	5.00mm×4.40mm×1.20mm	GT74LVC02 XXXXXXX	3	Tape and Reel,4000

(1) For all available packages, please contact product sales.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4) "XXXXX" in Marking will be appeared as the batch code.

5 Device Summary, Pin and Packages(Continued)

Fig.5-1. GT74LVC02: PD (SOP14/SOIC-14) Package
GT74LVC02: TD (TSSOP14) Package
Table 5-2 Pin definition

Name	Pin		I/O	Description
	PD	TD		
1Y	1		O	Gate 1 Data Output
1A	2		I	Gate 1 Data Input
1B	3		I	Gate 1 Data Input
2Y	4		O	Gate 2 Data Output
2A	5		I	Gate 2 Data Input
2B	6		I	Gate 2 Data Input
GND	7		-	Ground
3A	8		I	Gate 3 Data Input
3B	9		I	Gate 3 Data Input
3Y	10		O	Gate 3 Data Output
4A	11		I	Gate 4 Data Input
4B	12		I	Gate 4 Data Input
4Y	13		O	Gate 4 Data Output
VCC	14		-	Supply Voltage

6 Voltage, Temperature, ESD and Thermal ratings

6.1 Absolute Maximum Ratings⁽¹⁾

Parameters		Min.	Max.	Unit
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low State ⁽²⁾⁽³⁾	-0.5	V _{CC} +0.5	V
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature	-55	150	°C
T _{stg}	Storage temperature	-55	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

ESD		Value	Unit
V(ESD)	Electrostatic discharge	Human-body model (HBM) ⁽¹⁾	8 K
		Charged device model (CDM) ⁽²⁾	1.5 K

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6 Voltage, Temperature, ESD and Thermal Ratings(Continued)

6.3 Recommended Operating Conditions⁽¹⁾

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Min	Max	Units
V _{CC}	Supply Voltage	Operating	1.65	5.5	V
V _{IH}	High-Level Input Voltage	V _{CC} =1.65V to 1.95V	0.65×V _{CC}		V
		V _{CC} =2.3V to 2.7V	1.7		
		V _{CC} =3V to 3.6V	2		
		V _{CC} =4.5V to 5.5V	0.7×V _{CC}		
V _{IL}	Low-Level Input Voltage	V _{CC} =1.65V to 1.95V		0.35×V _{CC}	V
		V _{CC} =2.3V to 2.7V		0.7	
		V _{CC} =3V to 3.6V		0.8	
		V _{CC} =4.5V to 5.5V		0.3×V _{CC}	
V _I	Input Voltage		0	5.5	V
V _O	Output Voltage		0	V _{CC}	V
I _{OH}	High-Level Output Current	V _{CC} =1.65V		-4	mA
		V _{CC} =2.3V		-8	
		V _{CC} =3V		-16	
		V _{CC} =3V		-24	
I _{OL}	Low-Level Output Current	V _{CC} =4.5V		-32	mA
		V _{CC} =1.65V		4	
		V _{CC} =2.3V		8	
		V _{CC} =3V		16	
Δt/Δv	Input Transition Rise or Fall Rate	V _{CC} =1.8V±0.15V, 2.5V±0.2V		20	ns/V
		V _{CC} =3.3V±0.3V		10	
		V _{CC} =5V±0.5V		5	
TA	Operating Free-air Temperature	All Other Packages	-40	125	°C

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

6.4 Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
TSSOP-14	180	35	°C/W
SOP-14(SOIC-14)	120	36	°C/W

7 Electrical Specifications

7.1 Electrical Characteristics

$V_{CC}=1.65V$ to $5.5V$, FULL= $-40^{\circ}C$ to $+125^{\circ}C$. Typical values are at $T_A=+25^{\circ}C$ (unless otherwise noted)⁽¹⁾

Parameter	Symbol	Test Conditions	V_{CC}	TA	Min	Typ	Max	Units
Output								
Output High Voltage	V_{OH}	$I_{OH}=-100\mu A$	1.65V to 5.5V	FULL	$V_{CC}-0.1$			V
		$I_{OH}=-4mA$	1.65V	FULL	1.2			V
		$I_{OH}=-8mA$	2.3V	FULL	1.9			V
		$I_{OH}=-16mA$	3V	FULL	2.4			V
		$I_{OH}=-24mA$		FULL	2.3			V
		$I_{OH}=-32mA$	4.5V	FULL	3.8			V
Output Low Voltage	V_{OL}	$I_{OL}=100\mu A$	1.65V to 5.5V	FULL			0.1	V
		$I_{OL}=4mA$	1.65V	FULL			0.45	V
		$I_{OL}=8mA$	2.3V	FULL			0.3	V
		$I_{OL}=16mA$	3V	FULL			0.4	V
		$I_{OL}=24mA$		FULL			0.55	V
		$I_{OL}=32mA$	4.5V	FULL			0.55	V
Off-State Current	I_{off}	V_I or $V_O=5.5V$	0V	FULL			± 40	μA
Input								
Input Leakage Current	I_I	$V_I=5.5V$ or GND	0V to 5.5V	FULL			± 20	μA
Input Capacitance	C_i	$V_I=V_{CC}$ or GND	3.3V	FULL		5		pF
Power Supply								
Power Supply Range	V_{CC}		1.65V to 5.5V	FULL	1.65		5.5	V
Power Supply Current	I_{CC}	$V_I=V_{CC}$ or GND, $I_O=0$	5.5V	FULL			40	μA
Delta Power Current	ΔI_{CC}	One Input at $V_{CC}-0.6V$, Other Inputs at V_{CC} or GND	3V to 5.5V	FULL			5000	μA

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

7.2 Switching Characteristics

Over recommended operating free-air temperature range, $C_L=30pF$ or $50pF$ (unless otherwise noted)

Parameter	From(Input)	To(Output)	$-40^{\circ}C$ to $+125^{\circ}C$								Units
			$V_{CC}=1.8V\pm 0.15V$		$V_{CC}=2.5V\pm 0.2V$		$V_{CC}=3.3V\pm 0.3V$		$V_{CC}=5V\pm 0.5V$		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A or B	Y	1	9	1	3.8	1	4	1	3.3	ns

7.3 Operating Characteristics

$T_A=-40^{\circ}C$ to $+125^{\circ}C$

Parameter		Test Conditions	$V_{CC}=1.8V$	$V_{CC}=2.5V$	$V_{CC}=3.3V$	$V_{CC}=5V$	Units
			Typ	Typ	Typ	Typ	
C_{pd}	Power Dissipation Capacitance	$f=10MHz$	23	23	23	31	pF

8 Typical Characteristics

$V_{CC}=1.65V$ or $5.5V$, FULL= $-40^{\circ}C$ to $+125^{\circ}C$. Typical values are at $T_A=+25^{\circ}C$ (unless otherwise noted)

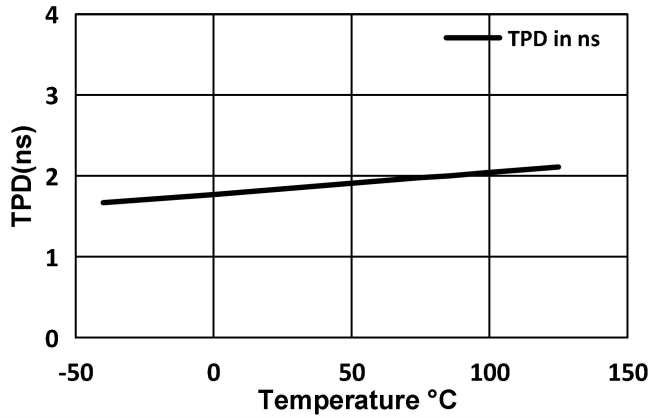


Fig.8-1. TPD Across Temperature at 3.3V V_{CC}

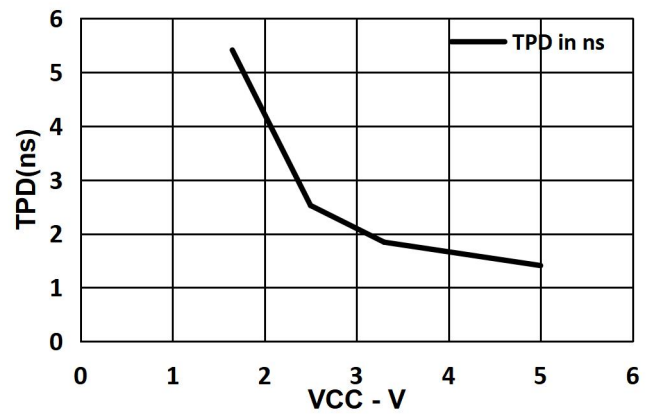
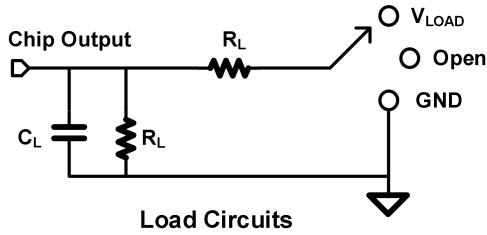


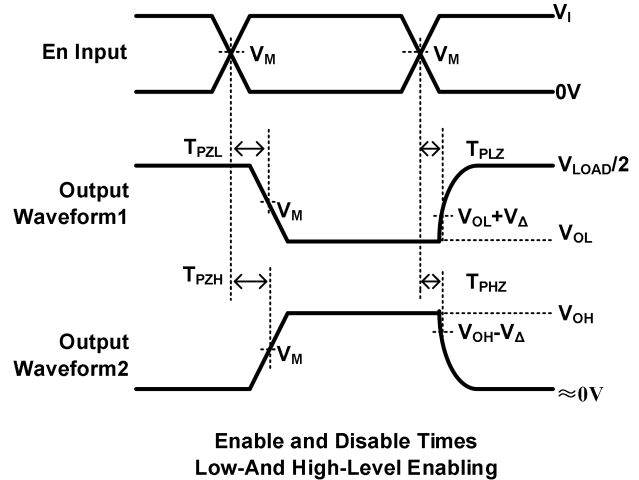
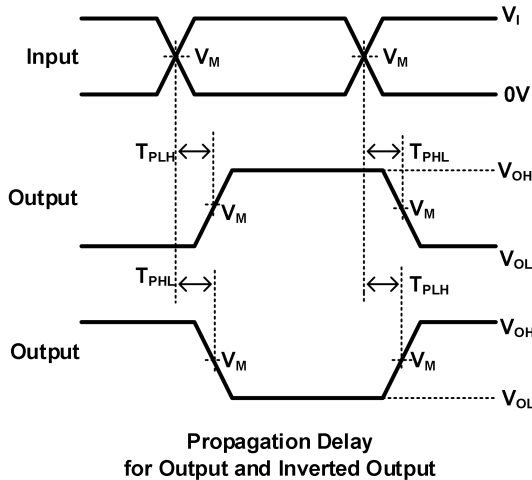
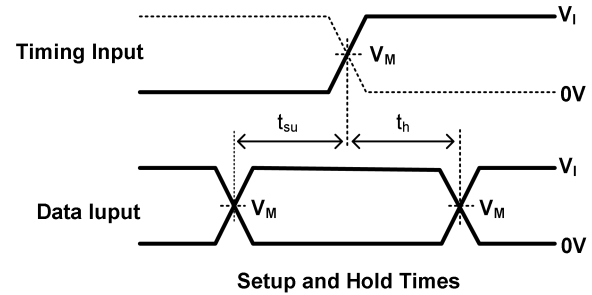
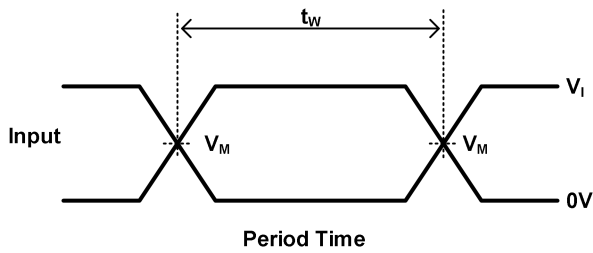
Fig.8-2. TPD Across V_{CC} at 25°C

9 Measurement Information



TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_i	T_r/T_f					
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1k Ω	0.15V
$2.5V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 Ω	0.15V
$3.3V \pm 0.15V$	3V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$5V \pm 0.15V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	50pF	500 Ω	0.3V



Notes:A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 .

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices.

10 Detailed Description

10.1 Overview

The GT74LVC02 device contains four 2-input positive-NOR gates and each gate performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

10.2 Functional Block Diagram

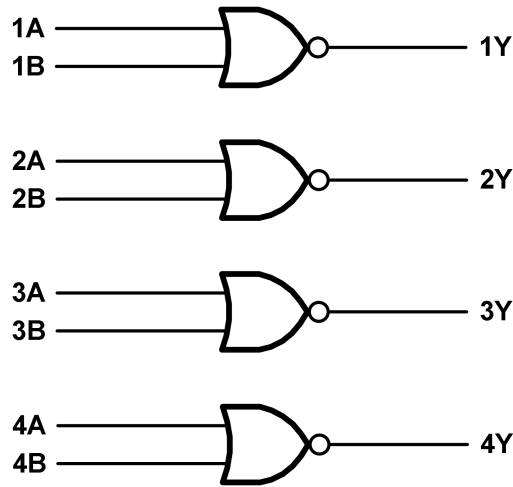


Fig.10-1.Functional Block Diagram

10.3 Feature Description

- Wide operating voltage range.
- Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

10.4 Device Functional Modes

Input A		Output Y	
A	B	Y	
H	X	L	
X	H	L	
L	L	H	

11 Application Note

The GT74LVC02 is a high drive CMOS device that can be used for implement NOR logic with a high output drive, such as an LED application. It can produce 24-mA of drive current at 3.3V making it Ideal for driving multiple outputs and good for high speed applications up to 100Mhz. The inputs are 5.5-V tolerant allowing translation down to V_{CC} .

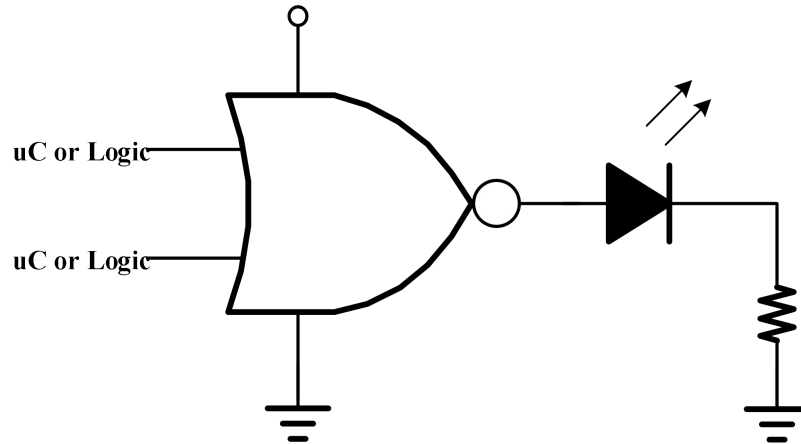
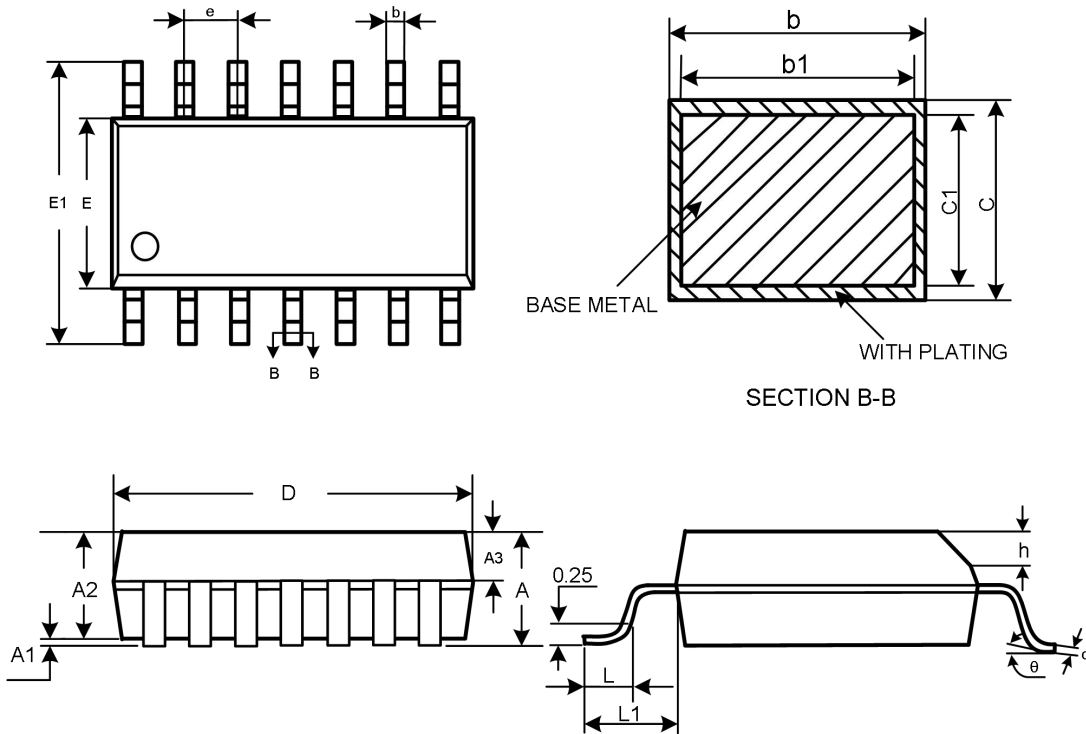


Fig.11-1. Basic LED Driver

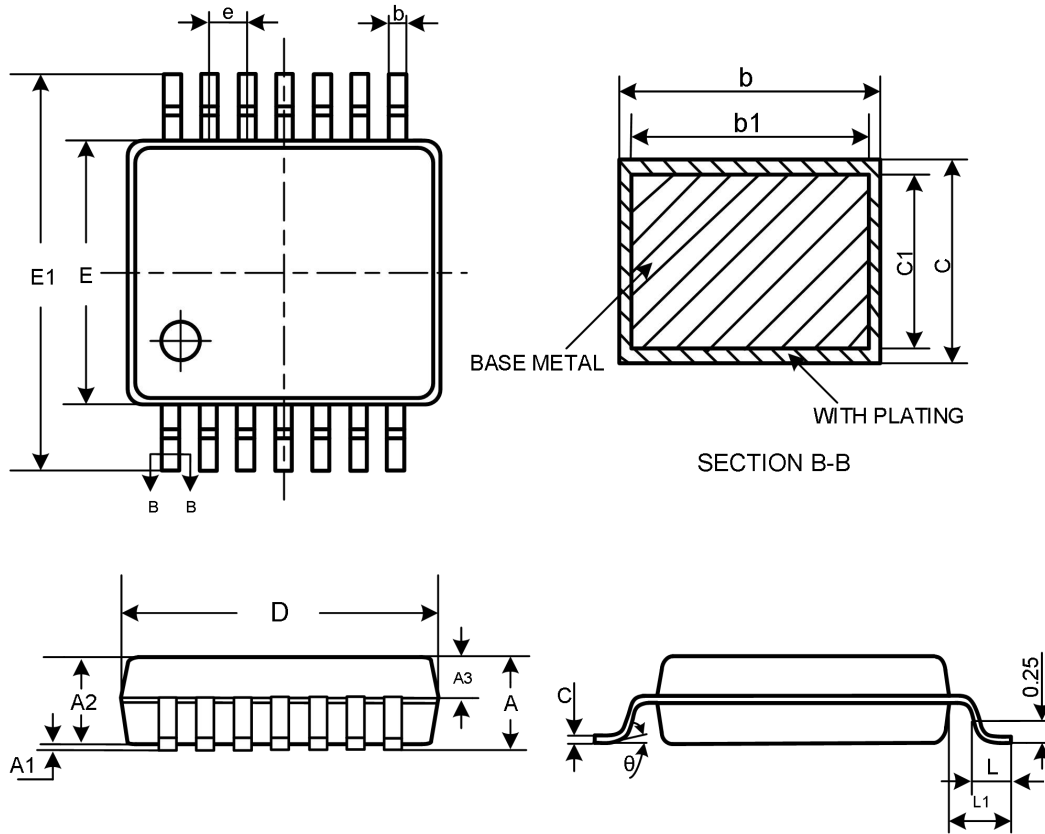
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μF capacitor is recommended. If there are multiple VCC pins, then a 0.01- μF or 0.022- μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Package Outline Dimension

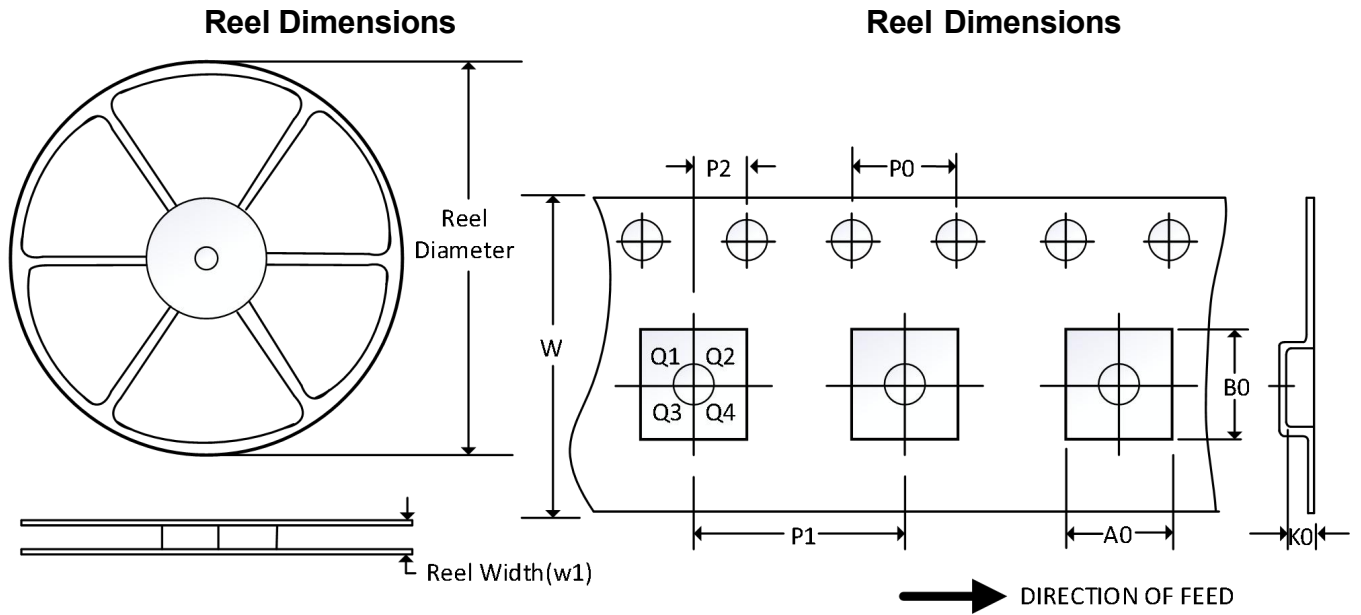
SOP14


Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.750	—	—	0.069
A1	0.100	—	0.225	0.004	—	0.009
A2	1.300	1.400	1.500	0.051	0.055	0.059
A3	0.600	0.650	0.700	0.024	0.026	0.028
b	0.390	—	0.470	0.015	—	0.019
b1	0.380	0.410	0.440	0.015	0.016	0.017
c	0.200	—	0.240	0.008	—	0.009
c1	0.190	0.200	0.210	0.007	0.008	0.008
D	8.550	8.650	8.750	0.337	0.341	0.344
E	5.800	6.000	6.200	0.228	0.236	0.244
E1	3.800	3.900	4.000	0.150	0.154	0.157
e	1.270BSC			0.050BSC		
h	0.250	—	0.500	0.010	—	0.020
L	0.500	—	0.800	0.020	—	0.031
L1	1.050REF			0.041REF		
θ	0°	—	8°	0°	—	8°

12 Package Outline Dimension(Continued)
TSSOP14


Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.200	—	—	0.047
A1	0.050	—	0.150	0.002	—	0.006
A2	0.900	1.000	1.050	0.035	0.039	0.041
A3	0.390	0.440	0.490	0.015	0.017	0.019
b	0.200	—	0.280	0.008	—	0.011
b1	0.190	0.220	0.250	0.007	0.009	0.010
c	0.130	—	0.170	0.005	—	0.007
c1	0.120	0.130	0.140	0.005	0.005	0.006
D	4.900	5.000	5.100	0.193	0.197	0.201
E1	4.300	4.400	4.500	0.169	0.173	0.177
E	6.200	6.400	6.600	0.244	0.252	0.260
e	0.650BSC			0.026BSC		
L	0.450	0.600	0.750	0.018	0.024	0.030
L1	1.000BCS			0.039BSC		
θ	0°	—	8°	0°	—	8°

13 Tape and Reel Information



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-14 (SOP14)	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.