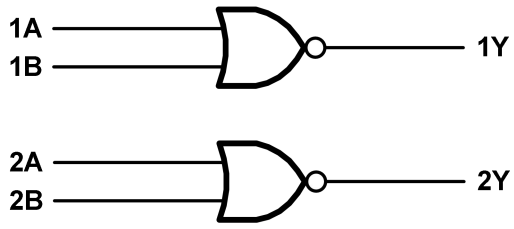
GT74LVC2G02
Dual 2-Input Positive-NOR Gate

1 Features	2 Application
- Operate from 1.65 V to 5.5 V - Supports 5-V VCC operation - Specified from -40°C to 125°C - Provides down translation to V_{CC} - Max t_{pd} of 4ns at 3.3 V - ±24-mA output drive at 3.3 V	- Personal digital assistant devices - AV receiver - MP3 player/recorder - Solid state drive (SSD): client and enterprise - Power: telecom/server AC/DC supply - TV: LCD/digital and high-definition (HDTV)

3 Description	Circuit Diagram
This dual 2-input positive-NOR gate is designed for 1.65-V to 5.5-V V_{CC} operation. The GT74LVC2G02 device performs the Boolean function $Y=\overline{A+B}$ or $Y=\overline{A}\cdot\overline{B}$ in positive logic. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when the gate is powered down and its output is floating.	

4 Revision History

Revision	Date	Note
Rev. A1. 0	2023. 09. 02	Original Version
Rev. A1. 1	2023. 12. 15	1.Updated Package Qty 2.Added Tape and Reel Information 3.Added Application Note
Rev. A1. 2	2023. 12. 26	1.Added Marking 2.Added MSL
Rev. A1. 3	2024. 01. 26	Updated Part Name

The latest datasheet version should be checked on the GTIC official website, as the company does not actively inform customers about updates to the datasheet.

5 Device Summary, Pin and Packages

Table 5-1. Device Summary(1)

Serial Name	Part Name	Package	Body Size (Nom)	Marking(2)(4)	MSL(3)	Package Qty
GT74LVC2G02	GT74LVC2G02V8	VSSOP8	2.00mm×2.30mm×0.75mm	2G02 XXXX	3	Tape and Reel,3000

(1) For all available packages, please contact product sales.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4) "XXXXX" in Marking will be appeared as the batch code.

5 Device Summary, Pin and Packages(Continued)

Top View

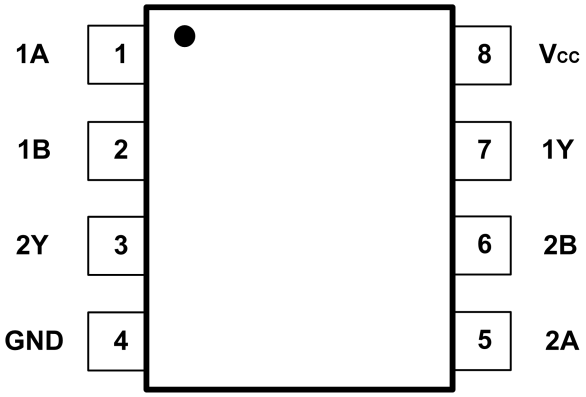


Fig.5-1. GT74LVC2G02: V8 (VSSOP8) Package

Table 5-2 Pin definition

Pin		I/O	Description
Name	V8		
1A	1	I	Gate 1 Data Input
1B	2	I	Gate 1 Data Input
2Y	3	O	Gate 2 Data Output
GND	4	-	Ground
2A	5	I	Gate 2 Data Input
2B	6	I	Gate 2 Data Input
1Y	7	O	Gate 1 Data Output
VCC	8	-	Supply Voltage

6 Voltage, Temperature, ESD and Thermal Ratings

6.1 Absolute Maximum Ratings(1)

Parameters			Min.	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low State(2)(3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-55	150	℃
T_{stg}	Storage temperature		-55	150	℃

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic discharge	Human-body model (HBM)(1)	8 K	V
		Charged device model (CDM)(2)	1.5 K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6 Voltage, Temperature, ESD and Thermal Ratings(Continued)

6.3 Recommended Operating Conditions(1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	1.65	5.5	V
V_{IH}	High-Level Input Voltage	V_{CC}=1.65V to 1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
V_{IL}	Low-Level Input Voltage	V_{CC}=1.65V to 1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-Level Output Current	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
I_{OL}	Low-Level Output Current	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Δt/Δv	Input Transition Rise or Fall Rate	V_{CC}=1.8V±0.15V, 2.5V±0.2V		20	ns/V
		V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
TA	Operating Free-air Temperature	All Other Packages	-40	125	°C

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

6.4 Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
VSSOP8	204	77	°C/W

7 Electrical Specifications

7.1 Electrical Characteristics

V_{CC}=1.65V to 5.5V, FULL=–40°C to +125°C. Typical values are at TA=+25°C (unless otherwise noted)(1)

Parameter	Symbol	Test Conditions	V_{CC}	TA	Min	Typ	Max	Units
Output								
Output High Voltage	V_{OH}	I_{OH}=–100μA	1.65V to 5.5V	FULL	V_{CC}-0.1			V
		I_{OH}=–4mA	1.65V	FULL	1.2			V
		I_{OH}=–8mA	2.3V	FULL	1.9			V
		I_{OH}=–16mA	3V	FULL	2.4			V
		I_{OH}=–24mA		FULL	2.3			V
		I_{OH}=–32mA	4.5V	FULL	3.8			V
Output Low Voltage	V_{OL}	I_{OL}=100μA	1.65V to 5.5V	FULL			0.1	V
		I_{OL}=4mA	1.65V	FULL			0.45	V
		I_{OL}=8mA	2.3V	FULL			0.3	V
		I_{OL}=16mA	3V	FULL			0.4	V
		I_{OL}=24mA		FULL			0.55	V
		I_{OL}=32mA	4.5V	FULL			0.55	V
Off-State Current	I_{off}	V_I or V_O=5.5V	0V	FULL			±10	μA
Input								
Input Leakage Current	I_I	V_I=5.5V or GND	0V to 5.5V	FULL			±5	μA
Input Capacitance	C_I	V_I=V_{CC} or GND	3.3V	FULL		5		pF
Power Supply								
Power Supply Range	V_{CC}		1.65V to 5.5V	FULL	1.65		5.5	V
Power Supply Current	I_{CC}	V_I=V_{CC} or GND, I_O=0	5.5V	FULL			10	μA
Delta Power Current	ΔI_{CC}	One Input at V_{CC} – 0.6V, Other Inputs at V_{CC} or GND	3V to 5.5V	FULL			500	μA

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

7.2 Switching Characteristics

Over recommended operating free-air temperature range,C_L=30pF or 50 pF (unless otherwise noted)

Parameter	From(Input)	To(Output)	–40°C to +125°C								Units
			V_{CC}=1.8V±0.15V		V_{CC}=2.5V±0.2V		V_{CC}=3.3V±0.3V		V_{CC}=5V±0.5V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A or B	Y	1	9	1	3.8	1	4	1	3.3	ns

7.3 Operating Characteristics

TA=–40°C to +125°C

Parameter		Test Conditions	V_{CC}=1.8V	V_{CC}=2.5V	V_{CC}=3.3V	V_{CC}=5V	Units
			Typ	Typ	Typ	Typ	
C_{pd}	Power Dissipation Capacitance	f=10Mhz	23	23	23	31	pF

8 Typical Characteristics

V_{CC}=1.65V or 5.5V, FULL=–40°C to +125°C. Typical values are at TA=+25°C (unless otherwise noted)

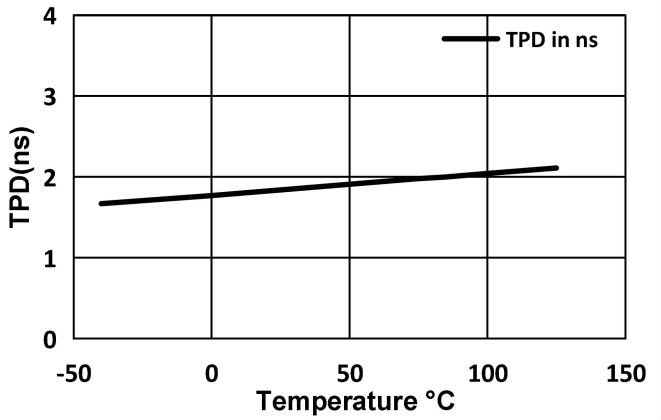


Fig.8-1. TPD Across Temperature at 3.3V V_{CC}

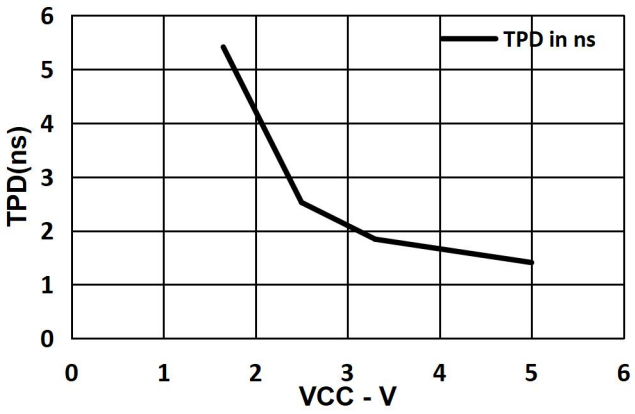
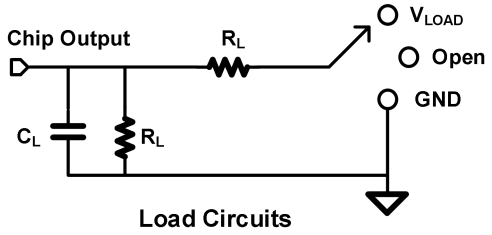


Fig.8-2. TPD Across V_{CC} at 25℃

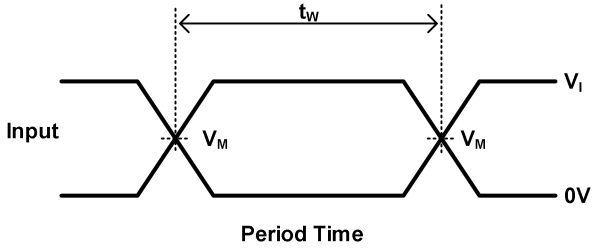
9 Measurement Information



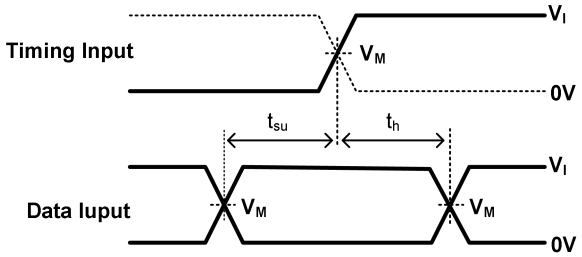
Load Circuits

TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

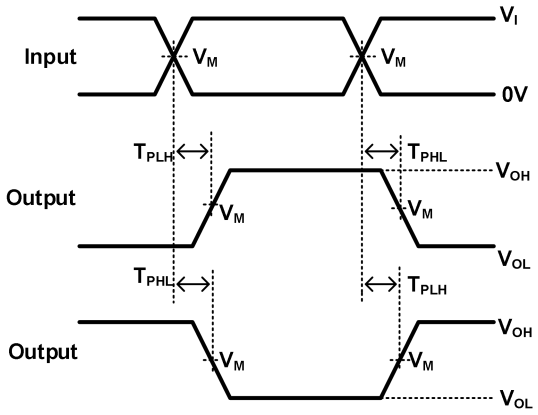
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1kΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V



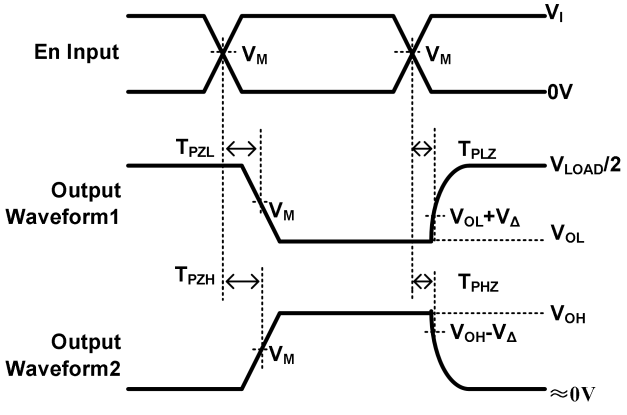
Period Time



Setup and Hold Times



Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 .
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

10 Detailed Description

10.1 Overview

The GT74LVC2G02 device contains two 2-input positive-NOR gates and each gate performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

10.2 Functional Block Diagram

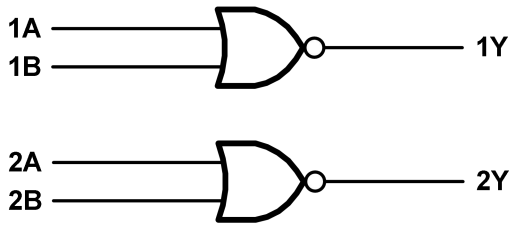


Fig.10-1.Functional Block Diagram

10.3 Feature Description

- Wide operating voltage range.
- Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

10.4 Device Functional Modes

Input		Output
A	**B**	**Y**
H	X	L
X	H	L
L	L	H

11 Application Note

The GT74LVC2G02 is a high drive CMOS device that can be used for implement NOR logic with a high output drive, such as an LED application. It can produce 24-mA of drive current at 3.3V making it Ideal for driving multiple outputs and good for high speed applications up to 100Mhz. The inputs are 5.5-V tolerant allowing translation down to V_{CC}.

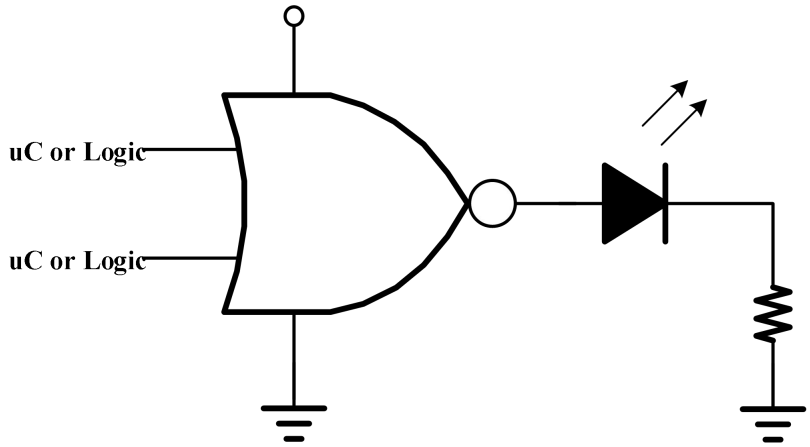


Fig.11-1. Basic LED Driver

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple VCC pins, then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

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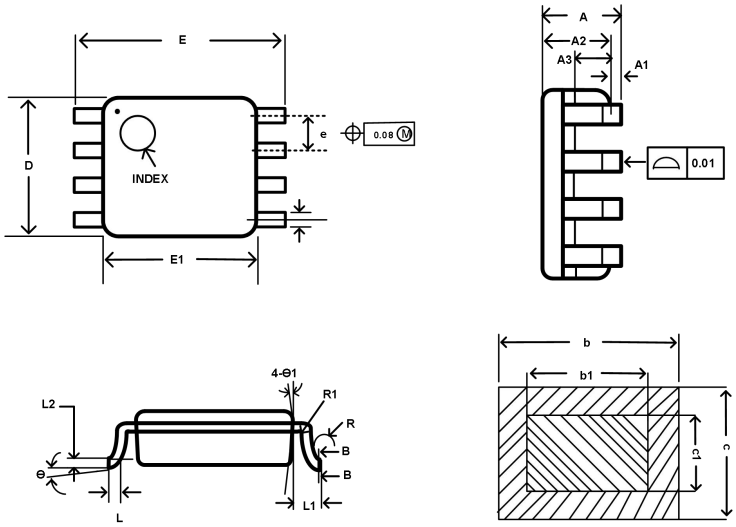
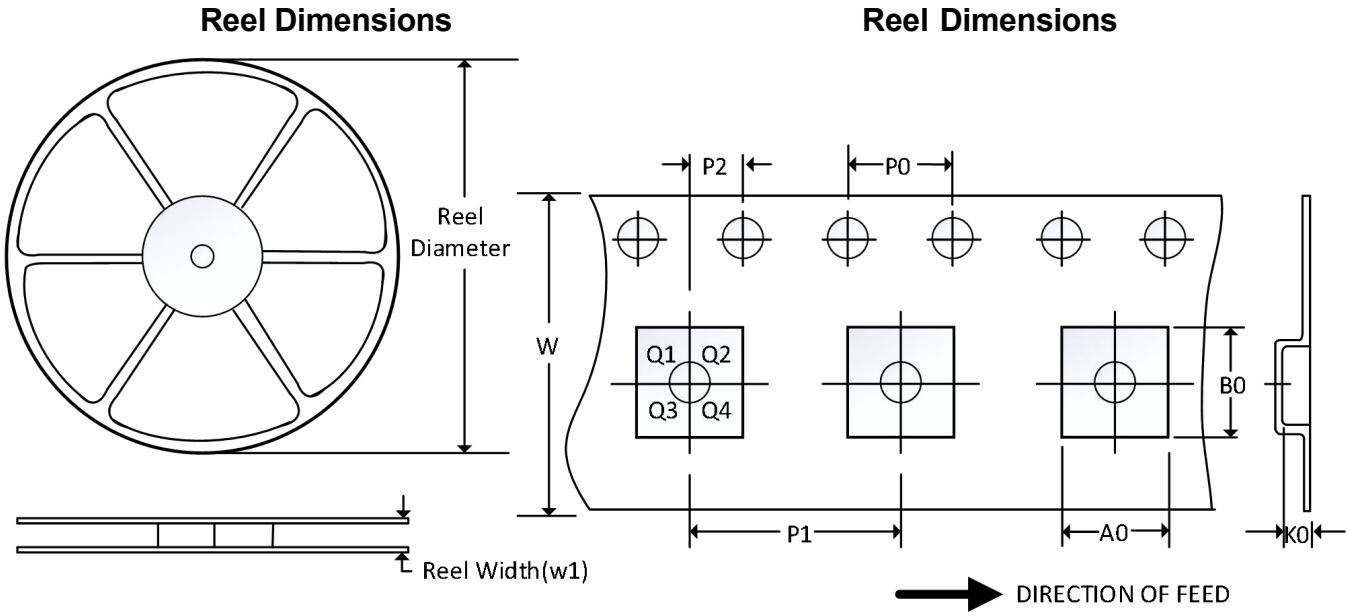
12 Package Outline Dimension

VSSOP8



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.90	-	-	0.035
A1	0	0.05	0.10	0.000	0.002	0.004
A2	0.65	0.75	0.80	0.026	0.030	0.031
A3	0.32	0.37	0.42	0.013	0.015	0.017
b	0.17	-	0.27	0.007	-	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	-	0.18	0.004	-	0.007
c1	0.10	0.13	0.14	0.004	0.005	0.006
E	3.00	3.10	3.20	0.118	0.122	0.126
D	1.90	2.00	2.10	0.075	0.079	0.083
E	3.00	3.10	3.20	0.118	0.122	0.126
E1	2.20	2.30	2.40	0.087	0.091	0.094
e	0.40	0.50	0.60	0.016	0.020	0.024
L	0.20	0.26	0.35	0.008	0.010	0.014
L1	0.40REF			0.016REF		
L2	0.12BSC			0.005BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
θ	0°	-	6°	0°	-	6°
θ1	9°	12°	15°	9°	12°	15°

13 Tape and Reel Information



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP8	7''	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.